

V_{DRM}	= 5600	V	Phase Control Thyristor 5STP 42U6500
V_{DSM}	= 6500	V	
$I_{T(AV)M}$	= 3460	A	
$I_{T(RMS)}$	= 5440	A	
I_{TSM}	= 71.4×10^3	A	
$V_{(T0)}$	= 1.24	V	
r_T	= 0.162	mW	

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- Patented free-floating silicon technology
- Low on-state and switching losses
- Designed for traction, energy and industrial applications
- Optimum power handling capability
- Interdigitated amplifying gate

Blocking

Maximum rated values ¹⁾

Symbol	Conditions	5STP 42U6500	5STP 42U6200	5STP 42U5800
V_{DSM}, V_{RSM}	$f = 5 \text{ Hz}, t_p = 10 \text{ ms}$	6500 V	6200 V	5800 V
V_{DRM}, V_{RRM}	$f = 50 \text{ Hz}, t_p = 10 \text{ ms}$	5600 V	5300 V	4900 V
V_{RSM}	$t_p = 5 \text{ ms}, \text{ single pulse}$	7000 V	6700 V	6300 V
dV/dt_{crit}	Exp. to 3750 V, $T_{vj} = 110^\circ\text{C}$	2000 V/ μs		

Characteristic values

Parameter	Symbol	Conditions	min	typ	max	Unit
Forward leakage current	I_{DSM}	$V_{DSM}, T_{vj} = 110^\circ\text{C}$			700	mA
Reverse leakage current	I_{RSM}	$V_{RSM}, T_{vj} = 110^\circ\text{C}$			700	mA

Mechanical data

Maximum rated values ¹⁾

Parameter	Symbol	Conditions	min	typ	max	Unit
Mounting force	F_M		120	135	160	kN
Acceleration	a	Device unclamped			50	m/s^2
Acceleration	a	Device clamped			100	m/s^2

Characteristic values

Parameter	Symbol	Conditions	min	typ	max	Unit
Weight	m				3.6	kg
Housing thickness	H	$F_M = 135 \text{ kN}, T_a = 25^\circ\text{C}$	34.8		35.5	mm
Surface creepage distance	D_S		56			mm
Air strike distance	D_a		22			mm

1) Maximum rated values indicate limits beyond which damage to the device may occur

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On-state

Maximum rated values ¹⁾

Parameter	Symbol	Conditions	min	typ	max	Unit
Average on-state current	$I_{T(AV)M}$	Half sine wave, $T_c = 70^\circ\text{C}$			3460	A
RMS on-state current	$I_{T(RMS)}$				5440	A
Peak non-repetitive surge current	I_{TSM}	$t_p = 10\text{ ms}$, $T_{vj} = 110^\circ\text{C}$, $V_D = V_R = 0\text{ V}$			71.4×10^3	A
Limiting load integral	$I^2 t$				25.48×10^6	A^2s
Peak non-repetitive surge current	I_{TSM}	$t_p = 8.3\text{ ms}$, $T_{vj} = 110^\circ\text{C}$, $V_D = V_R = 0\text{ V}$			76.14×10^3	A
Limiting load integral	$I^2 t$				24.64×10^6	A^2s

Characteristic values

Parameter	Symbol	Conditions	min	typ	max	Unit
On-state voltage	V_T	$I_T = 3000\text{ A}$, $T_{vj} = 110^\circ\text{C}$			1.71	V
Threshold voltage	$V_{(TO)}$	$I_T = 2000\text{ A} - 6000\text{ A}$, $T_{vj} = 110^\circ\text{C}$			1.24	V
Slope resistance	r_T				0.162	$\text{m}\Omega$
Holding current	I_H	$T_{vj} = 25^\circ\text{C}$			200	mA
		$T_{vj} = 110^\circ\text{C}$			100	mA
Latching current	I_L	$T_{vj} = 25^\circ\text{C}$			900	mA
		$T_{vj} = 110^\circ\text{C}$			700	mA

Switching

Maximum rated values ¹⁾

Parameter	Symbol	Conditions	min	typ	max	Unit
Critical rate of rise of on-state current	di/dt_{crit}	$T_{vj} = 110^\circ\text{C}$, $I_{TRM} = 3000\text{ A}$, Cont. $f = 50\text{ Hz}$			250	$\text{A}/\mu\text{s}$
Critical rate of rise of on-state current	di/dt_{crit}	$V_D \leq 1880\text{ V}$, $I_{FG} = 2\text{ A}$, $t_r = 0.5\text{ }\mu\text{s}$ Cont. $f = 1\text{ Hz}$			1000	$\text{A}/\mu\text{s}$
Circuit-commutated turn-off time	t_q	$T_{vj} = 110^\circ\text{C}$, $I_{TRM} = 3000\text{ A}$, $V_R = 200\text{ V}$, $di_T/dt = -1\text{ A}/\mu\text{s}$, $V_D \leq 0.67 \cdot V_{DRM}$, $dV_D/dt = 20\text{ V}/\mu\text{s}$	800			μs

Characteristic values

Parameter	Symbol	Conditions	min	typ	max	Unit
Recovery charge	Q_{rr}	$T_{vj} = 110^\circ\text{C}$, $I_{TRM} = 3000\text{ A}$, $V_R = 200\text{ V}$, $di_T/dt = -1\text{ A}/\mu\text{s}$	4200		5200	μAs
Gate turn-on delay time	t_{gd}	$V_D = 0.4 \cdot V_{RM}$, $I_{FG} = 2\text{ A}$, $t_r = 0.5\text{ }\mu\text{s}$, $T_{vj} = 25^\circ\text{C}$			3	μs

Triggering

Maximum rated values ¹⁾

Parameter	Symbol	Conditions	min	typ	max	Unit
Peak forward gate voltage	V_{FGM}				12	V
Peak forward gate current	I_{FGM}				10	A
Peak reverse gate voltage	V_{RGM}				10	V
Average gate power loss	$P_{G(AV)}$		see Fig. 9			

Characteristic values

Parameter	Symbol	Conditions	min	typ	max	Unit
Gate-trigger voltage	V_{GT}	$T_{vj} = 25\text{ °C}$			2.6	V
Gate-trigger current	I_{GT}	$T_{vj} = 25\text{ °C}$			400	mA
Gate non-trigger voltage	V_{GD}	$V_D = 0.4 \times V_{DRM}$, $T_{vjmax} = 110\text{ °C}$	0.3			V
Gate non-trigger current	I_{GD}	$V_D = 0.4 \times V_{DRM}$, $T_{vjmax} = 110\text{ °C}$	10			mA

Thermal

Maximum rated values ¹⁾

Parameter	Symbol	Conditions	min	typ	max	Unit
Operating junction temperature range	T_{vj}				110	°C
Storage temperature range	T_{stg}		-40		140	°C

Characteristic values

Parameter	Symbol	Conditions	min	typ	max	Unit
Thermal resistance junction to case	$R_{th(j-c)}$	Double-side cooled $F_m = 120...160\text{ kN}$			4	K/kW
	$R_{th(j-c)A}$	Anode-side cooled $F_m = 120...160\text{ kN}$			8	K/kW
	$R_{th(j-c)C}$	Cathode-side cooled $F_m = 120...160\text{ kN}$			8	K/kW
Thermal resistance case to heatsink	$R_{th(c-h)}$	Double-side cooled $F_m = 120...160\text{ kN}$			0.8	K/kW
	$R_{th(c-h)}$	Single-side cooled $F_m = 120...160\text{ kN}$			1.6	K/kW

Analytical function for transient thermal impedance:

$$Z_{th(j-c)}(t) = \sum_{i=1}^n R_{th i} (1 - e^{-t/t_i})$$

i	1	2	3	4
$R_{th i}(\text{K/kW})$	2.695	0.814	0.330	0.162
$\tau_i(\text{s})$	0.9692	0.1332	0.0177	0.0042

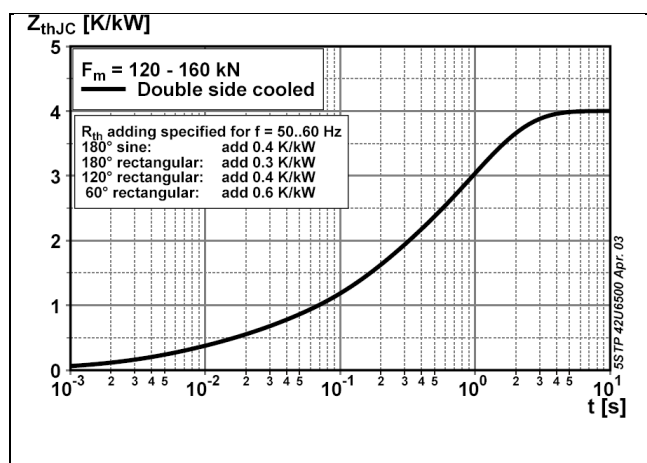
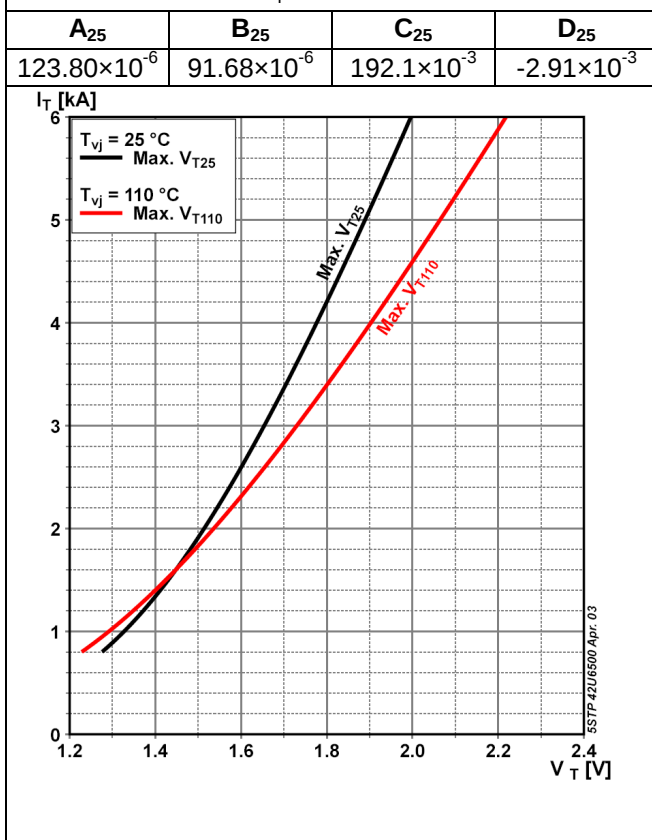


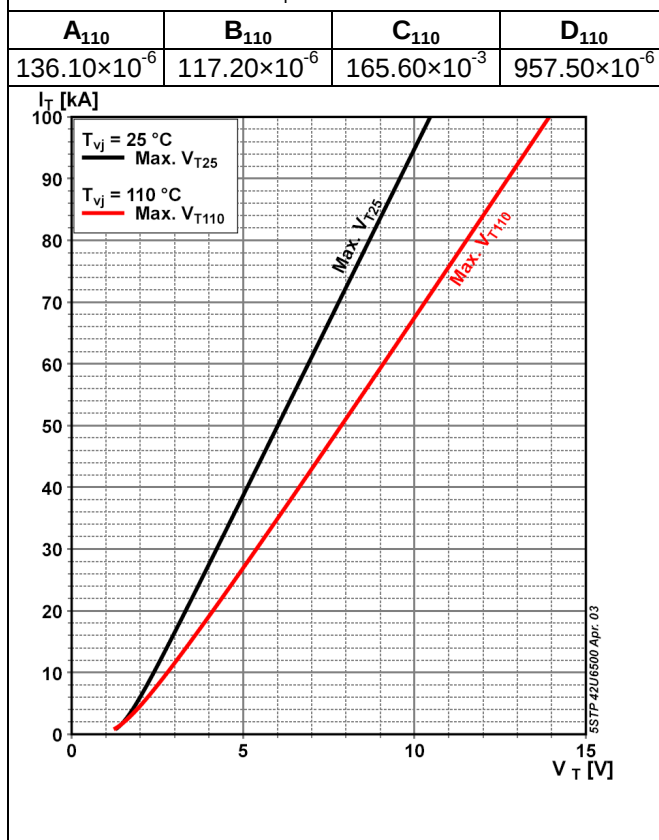
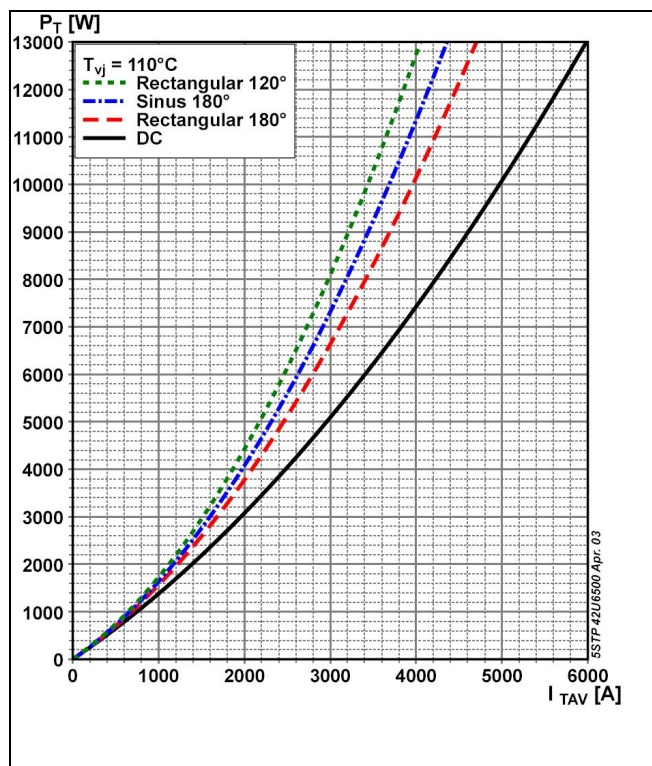
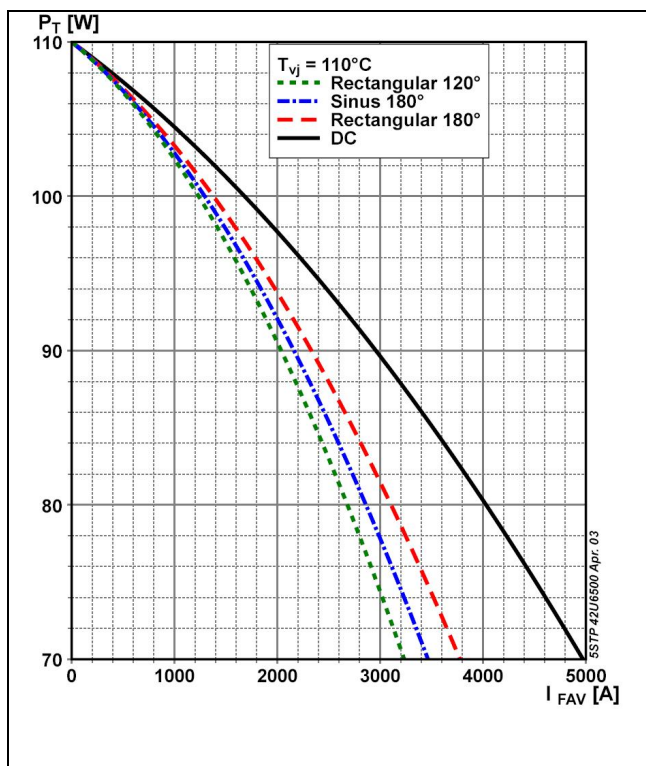
Fig. 1 Transient thermal impedance junction-to case.

Max. on-state characteristic model:

$$V_{T25} = A_{Tvj} + B_{Tvj} \cdot I_T + C_{Tvj} \cdot \ln(I_T + 1) + D_{Tvj} \cdot \sqrt{I_T}$$

Valid for $I_T = 800 - 100000$ A**Fig. 2** Max. on-state voltage characteristics**Max. on-state characteristic model:**

$$V_{T110} = A_{Tvj} + B_{Tvj} \cdot I_T + C_{Tvj} \cdot \ln(I_T + 1) + D_{Tvj} \cdot \sqrt{I_T}$$

Valid for $I_T = 800 - 100000$ A**Fig. 3** Max. on-state voltage characteristics**Fig. 4** On-state power dissipation vs. mean on-state current. Turn-on losses excluded.**Fig. 5** Max. permissible case temperature vs. mean on-state current.

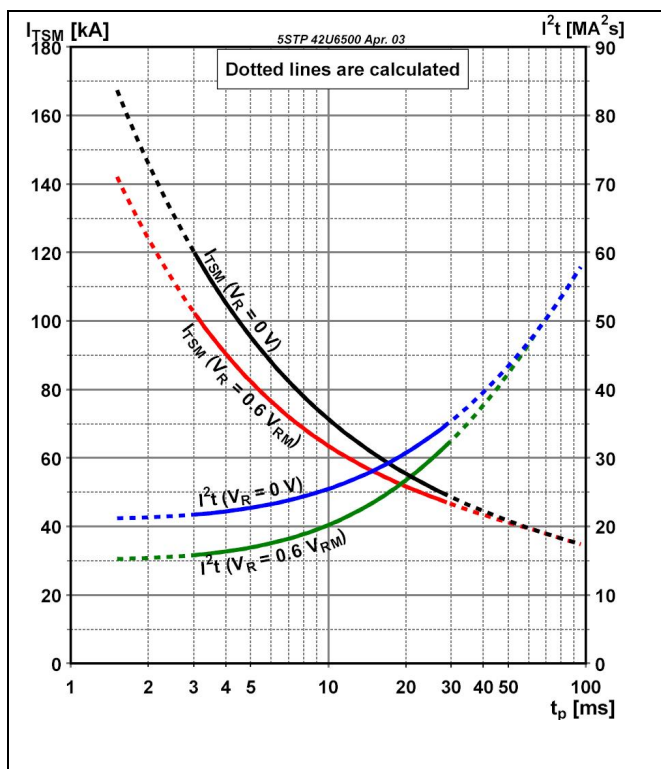


Fig. 6 Surge on-state current vs. pulse length. Half-sine wave.

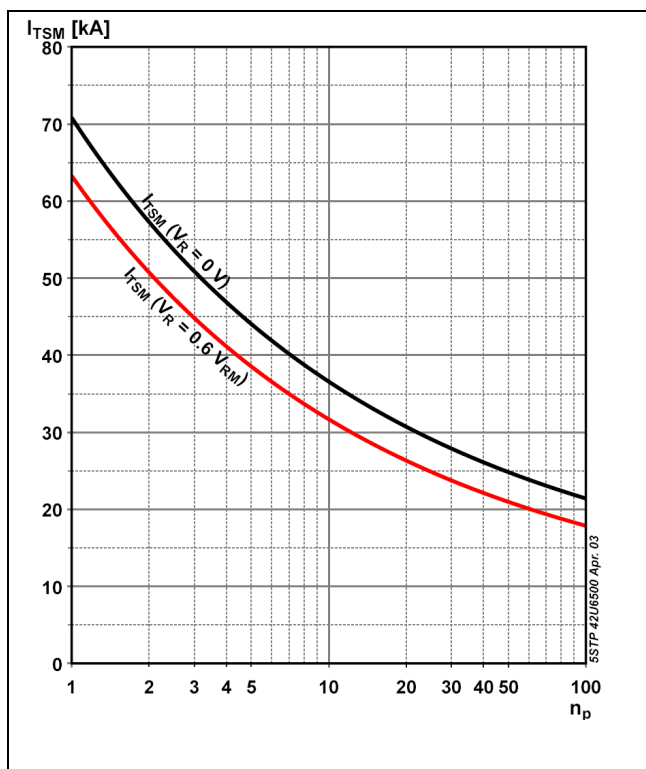


Fig. 7 Surge on-state current vs. number of pulses. Half-sine wave, 10 ms, 50Hz.

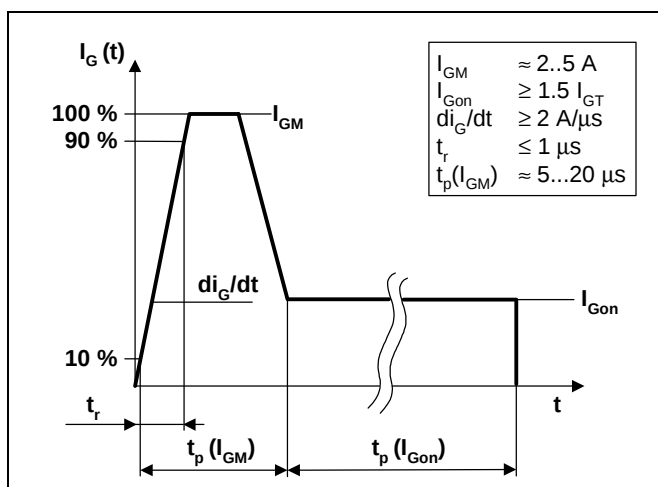


Fig. 8 Recommended gate current waveform.

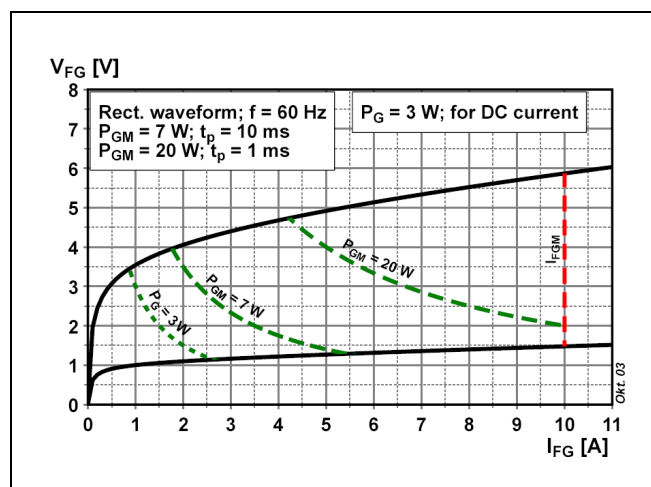


Fig. 9 Max. peak gate power loss.

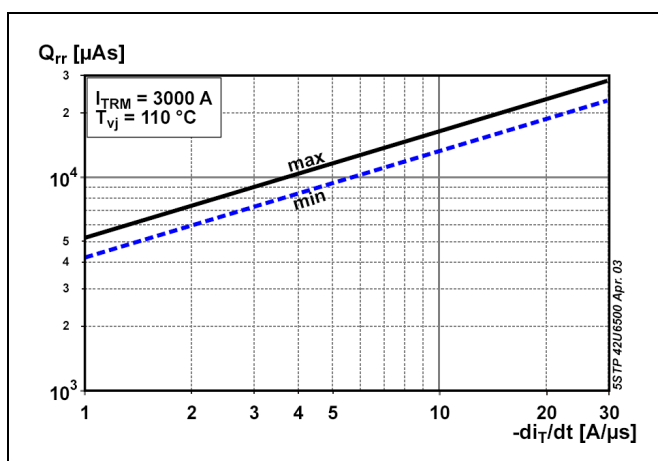


Fig. 10 Recovery charge vs. decay rate of on-state current.

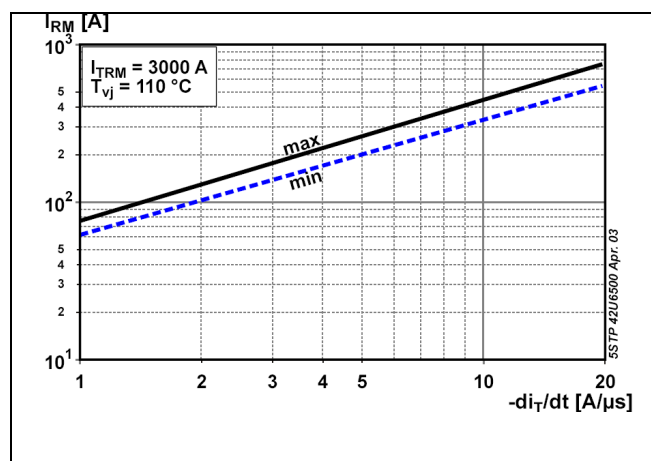


Fig. 11 Peak reverse recovery current vs. decay rate of on-state current.

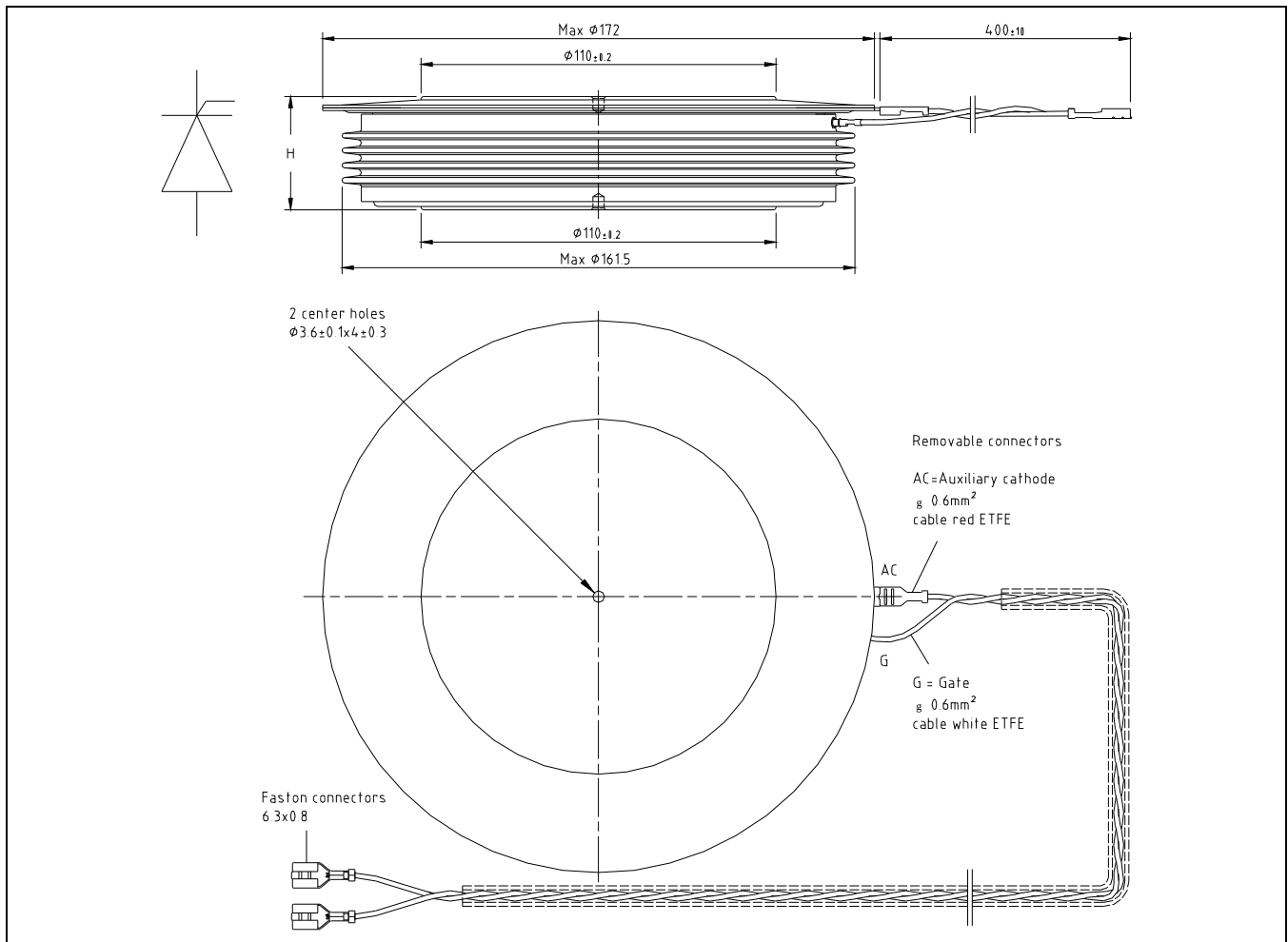


Fig. 12 Device Outline Drawing.

Related application notes:

Doc. Nr	Titel
5SYA2020	Design of RC-Snubber for Phase Control Applications
5SYA2034	Gate-drive Recommendations for PCT's
5SYA 2036	Recommendations regarding mechanical clamping of Press Pack High Power Semiconductors
Please refer to http://www.abb.com/semiconductors for actual versions.	

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